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WHAT IS CLAIMED IS:

| 1 | 1. A computer implemented method for selecting a code image during a |
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| 2 | reboot routine, comprising: |
| 3 | maintaining multiple code images in a memory device; |
| 4 | executing a first operation routine; |
| 5 | incrementing a first counter if the first operation routine succeeds; |
| 6 | executing a second operation routine; |
| 7 | incrementing a second counter if the second operation routine succeeds; and |
| 8 | using the first and second counters to select one of the code images from the |
| 9 | memory device to execute. |
| | |
| 1 | 2. The method of claim 1, further comprising: |
| 2 | designating one code image as non-operational if the first counter is a first value |
| 3 | and the second counter is a second value, wherein one other code image not designated as |
| 4 | non-operational is selected to execute. |
| | |
| 1 | 3. The method of claim 2, wherein the first value is greater than zero and the |
| 2 | second value is zero. |
| | |
| 1 | 4. The method of claim 2, further comprising: |
| 2 | receiving an update to the code image; |
| 3 | determining whether one code image is designated as non-operational; and |
| 4 | overwriting the code image designated as non-operational with the received |
| 5 | update to the code image if one code image is designated as non-operational. |
| | |
| 1 | 5. The method of claim 4, further comprising: |

determining an earliest version of the code images in the memory device; and

versions of the code image.

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| 3 | overwriting the determined earliest version of the code image if one code image is |
| 4 | not designated as non-operational. |
| 1 | 6. The method of claim 4, further comprising: |
| 2 | determining whether one code image is corrupted; and |
| 3 | if one code image is corrupted, overwriting the corrupted code image with the |
| 4 | received update before determining whether one code is non-operational. |
| 1 | 7. The method of claim 1, wherein the first operation routine comprises a |
| 2 | reboot routine and the second operation routine comprises an initialization routine. |
| | |
| 1 | 8. The method of claim 7, further comprising: |
| 2 | incrementing the second counter if the initialization routine successfully |
| 3 | completed; |
| 4 | rebooting if the initialization routine failed; and |
| 5 | performing another iteration of all previous steps after rebooting. |
| | |
| 1 | 9. The method of claim 7, further comprising: |
| 2 | selecting one copy of the code image, wherein the executed initialization routine |
| 3 | is a component of the selected code image, wherein the selected code image is designated |
| 4 | as non-operational if the first counter is the first value and the second counter is the |
| 5 | second value; and |
| 6 | selecting one other copy of the code image if the selected code image is |
| 7 | designated as non-operational. |
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| 1 | 10. The method of claim 1, wherein the code image comprise different |

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| 1 | 11. The method of claim 1, wherein the first operation routine comprises a |
| 2 | reboot routine and the second operation routine comprises an initialization routine, and |
| 3 | wherein the code images include a function routine to perform an operation after |
| 4 | initialization, further comprising: |
| 5 | executing the function routine in one code image; |
| 6 | incrementing a third counter associated with the code image including the |
| 7 | executed function routine if the function routine succeeded; and |
| 8 | using the third counter, in addition to the first and second counters, to select one |
| 9 | of the multiple copies of the code image from the memory device to execute. |
| | |
| 1 | 12. The method of claim 11, further comprising: |
| 2 | designating one code image as operational if the first, second, and third counters |
| 3 | satisfy at least one threshold value, wherein the code image designated as operational is |
| 4 | automatically selected from the memory device to execute after subsequent reboot |
| 5 | operations. |
| | |
| 1 | 13. The method of claim 11, further comprising: |
| 2 | designating one code/mage as non-operational if the first, second, and third |
| 3 | counters satisfy at least one threshold value, wherein one other code image not designated |
| 4 | as non-operational is selected from the memory device and executed. |
| | |
| 1 | 14. The method of claim 13, wherein the threshold value for the third counter |
| 2 | is zero and wherein the at least one threshold value for the first and second counters is |
| 3 | greater than zero |
| | |
| 1 | 15. The method of claim 13, further comprising: |
| 2 | incrementing the second counter if the initialization routine successfully |
| 3 | completed:/ |

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| 4 | rebooting if the initialization or function routine failed; and |
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| 5 | performing another iteration of all previous steps after rebooting. |
| | |
| 1 | 16. The method of claim 11, wherein the code image includes multiple |
| 2 | function routines, wherein there is one counter for each of the multiple function routines, |
| 3 | and further comprising: |
| 4 | designating one code image as operational if the first counter, second counter, and |
| 5 | each counter associated with a function routine satisfy at least one threshold value, |
| 6 | wherein the code image designated as operational is automatically selected from the |
| 7 | memory device to execute after subsequent reboot operations. |
| | |
| 1 | 17. The method of claim /, wherein one operation routine comprises one of a |
| 2 | reboot routine, an initialization routine or a function routine to perform a device specific |
| 3 | operation. |
| | |
| 1 | 18. A computer system for selecting a code image during a reboot routine, |
| 2 | comprising: |
| 3 | a processor; |
| 4 | a memory device maintaining multiple code images, wherein the processor is |
| 5 | capable of accessing them memory device; |
| 6 | program logic executed by the processor, wherein the program logic causes the |
| 7 | processor to perform: |
| 8 | (i) executing a first operation routine; |
| 9 | (ii) incrementing a first counter if the first operation routine succeeds; |
| 10 | executing a second operation routine; |
| 11 | (i/i) incrementing a second counter if the second operation routine |
| 12 | succeeds; and |
| | 1 |

| 13 | (iv) using the first and second counters to select one of the code images |
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| 14 | from the memory device to execute. |
| | |
| 1 | 19. The system of claim 18, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | designating one code image as non-operational if the first counter is a first value |
| 4 | and the second counter is a second value, wherein one other code image not designated as |
| 5 | non-operational is selected to execute. |
| 1 | 20. The system of claim 19, wherein the first value is greater than zero and the |
| 2 | second value is zero. |
| | |
| 1 | 21. The system of claim 19, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | receiving an update to the code image; |
| 4 | determining whether one code image is designated as non-operational; and |
| 5 | overwriting the code image designated as non-operational with the received |
| 6 | update to the code image if one code image is designated as non-operational. |
| | |
| 1 | 22. The system of claim 21, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | determining an earliest version of the code images in the memory device; and |
| 4 | overwriting the determined earliest version of the code image if one code image is |
| 5 | not designated as non-operational. |
| | |
| i | 23. The system of claim 21, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | determining whether one code image is corrupted; and |
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| 4 | if one code image is corrupted, overwriting the corrupted code image with the |
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| 5 | received update before determining whether one code is non-operational. |
| | |
| 1 | 24. The system of claim 18, wherein the first operation routine comprises a |
| 2 | reboot routine and the second operation routine comprises an initialization routine. |
| | |
| 1 | 25. The system of claim 24, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | incrementing the second counter if the initialization routine successfully |
| 4 | completed; |
| 5 | rebooting if the initialization routine failed; and |
| 6 | performing another iteration of all previous steps after rebooting. |
| | |
| 1 | 26. The system of claim 24, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | selecting one copy of the code image, wherein the executed initialization routine |
| 4 | is a component of the selected code image, wherein the selected code image is designated |
| 5 | as non-operational if the first counter is the first value and the second counter is the |
| 6 | second value; and |
| 7 | selecting one other copy of the code image if the selected code image is |
| 8 | designated as non-operational |
| | |
| 1 | 27. The system of claim 18, wherein the code image comprise different |
| 2 | versions of the code image. |
| | |
| 1 | 28. The system of claim 18, wherein the first operation routine comprises a |
| 2 | reboot routine and the second operation routine comprises an initialization routine, and |

wherein the code images include a function routine to perform an operation after

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| 4 | initialization, wherein the program logic is further capable of causing the processor to |
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| 5 | perform: |
| 6 | executing the function routine in one code image; |
| 7 | incrementing a third counter associated with the code image including the |
| 8 | executed function routine if the function routine succeeded; and |
| 9 | using the third counter, in addition to the first and second counters, to select one |
| 10 | of the multiple copies of the code image to from the memory device to execute. |
| 1 | 29. The system of claim 28, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | designating one code image as operational if the first, second, and third counters |
| 4 | satisfy at least one threshold value, wherein the code image designated as operational is |
| 5 | automatically selected from the memory device to execute after subsequent reboot |
| 6 | operations. |
| 1 | 30. The system of claim 28 wherein the program logic is further capable of |
| 2 | causing the processor to perform: |
| 3 | designating one code image as non-operational if the first, second, and third |
| 4 | counters satisfy at least one threshold value, wherein one other code image not designated |
| 5 | as non-operational is selected from the memory device and executed. |
| 1 | 31. The system of claim 30, wherein the threshold value for the third counter |
| 2 | is zero and wherein the at least one threshold value for the first and second counters is |
| 3 | greater than zero |
| 1 | 32. The system of claim 30, wherein the program logic is further capable of |
| 2 | causing the processor to perform: |

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incrementing the second counter if the initialization routine successfully 3 4 completed; rebooting if the initialization or function routine failed; and 5 performing another iteration of all previous steps after rebooting. 6 The system of claim 28, wherein the code image includes multiple 33. function routines, wherein there is one counter for each of the multiple function routines, 2 3 and further comprising: designating one code image as operational if the first counter, second counter, and 4 each counter associated with a function routine satisfy at least one threshold value, 5 wherein the code image designated as operational is automatically selected from the 6 memory device to execute after subsequent reboot operations. 7 The system of claim 18/wherein one operation routine comprises one of a 1 34. reboot routine, an initialization routine or a function routine to perform a device specific 2 3 operation. An article of manufacture for selecting a code image during a reboot 1 35. routine, wherein the article of manufacture includes code in a computer readable medium 2 capable of causing a processor to perform: 3 maintaining multiple/code images; 4 5 executing a first operation routine; incrementing a first counter if the first operation routine succeeds; 6 executing a second operation routine; 7 incrementing a second counter if the second operation routine succeeds; and 8

using the first and second counters to select one of the code images to execute.

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| 1 | 36. The article of manufacture of claim 35, wherein the article of manufacture |
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| 2 | code is further capable of causing the processor to perform: |
| 3 | designating one code image as non-operational if the first counter is a first value |
| 4 | and the second counter is a second value, wherein one other code image not designated as |
| 5 | non-operational is selected to execute. |
| 1 | 37. The article of manufacture of claim 36, wherein the first value is greater |
| 2 | than zero and the second value is zero. |
| 1 | 38. The article of manufacture of plaim 36, wherein the article of manufacture |
| 2 | code is further capable of causing the processor to perform: |
| 3 | receiving an update to the code image; |
| 4 | determining whether one code image is designated as non-operational; and |
| 5 | overwriting the code image designated as non-operational with the received |
| 6 | update to the code image if one code image is designated as non-operational. |
| 1 | 39. The article of manufacture of claim 38, wherein the article of manufacture |
| 2 | code is further capable of causing the processor to perform: |
| 3 | determining an earliest version of the code images; and |
| 4 | overwriting the determined earliest version of the code image if one code image is |
| 5 | not designated as non-operational. |
| 1 | 40. The article of manufacture of claim 38, wherein the article of manufacture |
| 2 | code is further capable of causing the processor to perform: |
| 3 | determining whether one code image is corrupted; and |
| 4 | if one code image is corrupted, overwriting the corrupted code image with the |
| 5 | received update before determining whether one code is non-operational. |
| | |

The article of manufacture of claim 35, wherein the first operation routine 1 41. comprises a reboot routine and the second operation routine comprises an initialization 2 3 routine. The article of manufacture of claim 41/wherein the article of manufacture 42. code is further capable of causing the processor to perform: 2 incrementing the second counter if the initialization routine successfully 3 4 completed; rebooting if the initialization routine faile, and 5 performing another iteration of all previous steps after rebooting. 6 The article of manufacture of claim 41, wherein the article of manufacture 1 43. code is further capable of causing the processor to perform: 2 selecting one copy of the code image, wherein the executed initialization routine 3 is a component of the selected code image, wherein the selected code image is designated 4 as non-operational if the first counter is the first value and the second counter is the 5 second value; and 6 7 selecting one other copy of the code image if the selected code image is designated as non-operational. 8 The article of manufacture of claim 35, wherein the code image comprise 44. 1 different versions of the code image. The article of manufacture of claim 35, wherein the first operation routine 45. 1 comprises a reboot routine and the second operation routine comprises an initialization routine, and wherein the code images include a function routine to perform an operation

after initialization, wherein the article of manufacture code is further capable of causing

the processor to perform

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executing the function routine in one code image/ 6 incrementing a third counter associated with the code image including the 7 executed function routine if the function routine succeeded; and using the third counter, in addition to the first and second counters, to select one 9 10 of the multiple copies of the code image to execute 1 46. The article of manufacture of claim 45, wherein the article of manufacture code is further capable of causing the processor to perform: 2 3 designating one code image as operational if the first, second, and third counters satisfy at least one threshold value, wherein the code image designated as operational is 4 automatically selected to execute after subsequent reboot operations. 5 The article of manufacture of claim 45, wherein the article of manufacture 1 47. code is further capable of causing the processor to perform: 2 designating one code image as non-operational if the first, second, and third 3 counters satisfy at least one threshold value, wherein one other code image not designated 4 as non-operational is selected and executed. 5 The article of manufacture of claim 47, wherein the threshold value for the 48. 1 third counter is zero and wherein the at least one threshold value for the first and second 2 counters is greater than zero 3 The article of manufacture of claim 47, wherein the article of manufacture 49. 1 code is further capable of causing the processor to perform: incrementing the second counter if the initialization routine successfully 3 4 completed; rebooting if the initialization or function routine failed; and 5 performing another iteration of all previous steps after rebooting. 6

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| l | 50. The article of manufacture of claim 45, wherein the code image includes |
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| 2 | multiple function routines, wherein there is one counter for each of the multiple function |
| 3 | routines, wherein the article of manufacture code is further capable of causing the |
| 1 | processor to perform: |
| 5 | designating one code image as operational if the first counter, second counter, and |
| | / |

- each counter associated with a function routine satisfy at least one threshold value, wherein the code image designated as operational is automatically selected to execute 7 after subsequent reboot operations. 8
- The article of manufacture of claim 35, wherein one operation routine 51. 1 comprises one of a reboot poutine, an initialization routine or a function routine to 2 perform a device specific operation.